In the Claims:

1. (Currently Amended) A method ~~Method~~ for operating an array of nonvolatile charge trapping memory devices, each device having a charge-trapping layer that traps charge by mitigating lateral charge transport therein, the method comprising:

in response to a block erase request and before block erasing the array by discharging substantially all of the non-volatile charge trapping memory devices of the array,

block programming the array by charging substantially all of the non-volatile charge trapping memory devices of the array, using the charge-trapping layer in each device to trap charge and mitigate lateral charge transport therein.

2. (Currently Amended) A method ~~Method~~ according to claim 1, furthermore comprising ~~after the erase operation~~ programming some of the non-volatile memory devices of the array after the erase operation based ~~depending~~ on data content to be stored in the non-volatile memory devices of the array.

3. (Currently Amended) A method ~~Method~~ according to claim 2, furthermore comprising reading the data content stored in a non-volatile memory device of the array using ~~, wherein for reading the data content stored in a non-volatile memory device of the array~~ at least one further non-volatile memory device having a dielectric charge trapping layer ~~is used~~ as reference cell, the dielectric charge trapping layer having a crystalline structure that traps the charge at energy minima therein by mitigating lateral charge transport within the trapping layer, and programming and erasing the dielectric charge trapping layer ~~which is programmed and erased~~ for a block programming and block erase, respectively, of the non-volatile memory devices in the array.

4. (Currently Amended) A method ~~Method~~ according to claim 3, wherein

the memory devices of the array together function as reference cells, and

discharging substantially all of the non-volatile charge trapping memory devices of the array includes discharging substantially all of the non-volatile charge trapping

memory devices in a discharging cycle, each subsequent discharging cycle being executed after an intervening charging cycle.

5. (Currently Amended) An electrical device comprising

an array of non-volatile charge trapping memory devices, each device having a charge-trapping layer that traps charge by mitigating lateral charge transport therein, and

a memory controller configured to

control block programming the array by charging substantially all of the non-volatile charge trapping memory devices of the array, using the charge-trapping layer to trap charge at a trapping location within the charge-trapping layer via the mitigation of lateral charge transport away from the trapping location,

control block erasing the array by discharging substantially all of the programmed non-volatile charge trapping memory devices of the array, and

control the array of non-volatile charge trapping memory devices such that, in response to a block erase request and before block erasing of substantially all of the non-volatile memory devices of the array, substantially all of the non-volatile memory devices of the array are block programmed.

6. (Previously presented) An electrical device according to claim 5, wherein the non-volatile memory device comprises a transistor having a channel and a control gate, a dielectric charge trapping layer being located between the channel and the control gate.

7. (Previously presented) An electrical device according to claim 5, the array being provided with at least one non-volatile memory device for use as a reference cell in a sense amplifier.

8. (Previously presented) An electrical device according to claim 7, the array comprising circuitry configured to program and erase the reference cell for a block-programming and block-erasing respectively of the non-volatile memory devices in the array.

9. (Previously presented) An electrical device according to claim 7, wherein the at least one reference cell is separate from the array.

10. (Previously presented) An electrical device according to claim 7, wherein the memory devices of the array are configured to function as reference cells.

11. (Previously presented) An electrical device according to claim 7, comprising circuitry configured compare a read current from a non-volatile memory device in the array with a read current from the reference cell.

12. (Previously presented) An electrical device according to claim 7, comprising circuitry configured to adapt a read current for reading the non-volatile memory devices in the array to the ageing of the reference cell.

13. (Previously presented) An electrical device according to claim 7, comprising circuitry configured to adapt a required control gate voltage for reading the non-volatile memory devices in the array depending on the ageing of the reference cell.

14. (Previously presented) An electrical device according to claim 5, wherein the array of non-volatile memory devices forms a non-volatile memory.

15. (Previously presented) A method according to claim 1, wherein the non-volatile memory devices of the array each include a dielectric charge trapping layer and wherein block programming the array by charging substantially all of the non-volatile charge trapping memory devices of the array includes trapping charge in the dielectric charge trapping layers.

16. (Currently Amended) A method for use with programming an array of non-volatile charge trapping memory devices according to data content to be stored therein, each device having a charge-trapping layer that traps charge by mitigating lateral charge transport therein, the method comprising, prior to substantially every programming step:

block programming, in response to a block erase request, substantially all of the non-volatile charge trapping memory devices of the array by charging substantially all of the non-volatile charge trapping memory devices, using the charge-trapping layer to trap charge therein by mitigating lateral charge transport within the charge-trapping layer; and

after the block programming step, block erasing substantially all of the non-volatile charge trapping memory devices of the array by discharging substantially all of the non-volatile charge trapping memory devices.

17. (Previously presented) The method of claim 16, further comprising programming a reference memory cell each time the block programming step is performed, and erasing the reference memory cell each time the block erasing step is performed, wherein the reference memory cell is a non-volatile charge trapping memory device.

18. (Previously presented) The method of claim 17, further comprising comparing a read current from a selected non-volatile memory device in the array with a read current from the reference memory cell.

19. (Previously presented) The method of claim 18, further comprising adapting the read current from the selected non-volatile memory device based on the read current from the reference memory cell.

20. (Previously presented) The method of claim 17, wherein the reference memory cell has a programming and erasing history that matches the block programming and blocking erasing history of the array.

21. (Previously presented) The method of claim 1, wherein the array is operated such that substantially none of the non-volatile charge trapping memory devices experiences two consecutive discharging cycles without experiencing an intermediate charging cycle.